REMARKS

Claims 1 - 4 are presently pending in the application. A reply under 37 C.F.R. § 1.116 was previously filed on May 16, 2003. In response to this reply, the Examiner mailed an Advisory Action on May 27, 2003, informing the Applicant that the rejections would stand as the Examiner believed the grounds of rejection to be proper.

On June 9, 2003, the Applicant's representative called the Examiner to discuss the rejection. During this discussion the Examiner noted the intricacy of the functional language of claims 1 and 3. It is upon this functional language, that stems from the structure of the instant invention as claimed, that Applicant respectfully requests further consideration.

Specifically, the prior art cited in the grounds of rejection fails to possess the structure and function of an adder circuit as claimed in independent claims 1 and 3. That is, U.S.P. No. 5,602,509 ("Kimura") discloses transistors M51, M52, M53 and M54 connected as a squaring circuit. This circuit arrangement prevents the Kimura reference from operating as an adder.

In other words, the aforementioned transistors and general arrangement of the Kimura reference prevents the Kimura reference from possessing a linear addition function at the common source of transistors M56 and M57 (node B) as required by independent claims 1 and 3 of the instant invention. Simply stated, the circuit of Kimura does not provide a linear addition output voltage $(V_1+V_2)/2$ as is required to anticipate the adder circuit claimed in this application.

I. Rejection Under 35 U.S.C. § 102(b)

Claims 1 - 4 stand rejected as allegedly being anticipated by U.S.P. No. 5,602,509 ("Kimura"). For the following reasons, this rejection is respectfully traversed.

Independent Claims 1 and 3

Independent claims 1 and 3 recite (among other things) a voltage adder circuit wherein the addition function derives at commonly coupled source electrodes of first and second MOS transistors. It is asserted that the prior art relied upon in the grounds of rejection (U.S.P. No. 5,602,509 ("Kimura")) fails to teach or suggest at least these elements of the independent claims.

The grounds of rejection compare the source electrodes of transistors M56 and M57 (coupled at node B in Figure 1) to the commonly coupled source electrodes of the instant invention. In response, it is respectfully averred that Kimura is not an adder circuit and cannot meet the limitations of the instant invention, as explained below.

In Fig. 1 of Kimura, transistors M51 - M54 constitute a squaring circuit. The circuit of Kimura operates linearly when $n=1+2/\sqrt{3}$ (=2.1547). That is, the following relation should be satisfied:

$$I_{DS6}+I_{DS7}=I_0+(1/2)\beta\, Vi^2 \quad (1)$$

where I_0 is a constant current.

By applying the current rule of Kirchhoff's law at node B, the following equation is obtained:

$$I_{DS6}+I_{DS7}+I_{DS5}=aI \quad (2)$$

By substituting formula (1) for formula (2), the following formula is obtained:

$$I_{DS5}=aI-I_0-(1/2)\beta\ Vi^2 \qquad (3)$$

where aI is greater than or equal to $I_0+(1/2)\beta\ Vi^2$.

Drain current I_{DS5} of transistor M55 is represented as follows:

$$I_{DS5}=\beta\ (V_A - V_B - V_{TH})^2 \qquad (4)$$

From formulae (3) and (4), the following relation is obtained:

$$V_A - V_B - V_{TH}= \sqrt{[(1/\beta)(aI - I_o)-(1/2)Vi^2]} \qquad (5)$$

Therefore, by substituting formula (6), i.e.:

$$V_B=(V_1+V_2)/2 - \sqrt{[I_o/(2\beta)]} - V_{TH} \qquad (6)$$

for formula (5), the following relation is obtained:

$$V_A = (V_1+V_2)/2 - \sqrt{[I_o/(2\beta)]} + \sqrt{[(1/\beta)(aI - I_O)-(1/2)Vi^2]} \qquad (7)$$

From formula (7), it is readily apparent that in the circuit of Fig. 1 of Kimura, the voltage of node A also includes a component: $\sqrt{[(1/\beta)(aI - I_o)-(1/2)Vi^2]}$ which varies depending on the differential input voltage.

Therefore, because the voltage at node A varies depending upon the differential input voltage, and due to the relationship between node A and node B, the circuit of Kimura fails to operate as an adder circuit. Simply stated, the circuit of Kimura does not provide a linear addition output voltage $(V_1+V_2)/2$ as is required to anticipate the function of an adder circuit as in the instant invention.

In light of the previous, it is averred that independent claims 1 and 3 recite features that are entirely absent in the prior art relied upon in the grounds of rejection. Accordingly, the Examiner is respectfully requested to reconsider and withdraw this anticipation rejection.

Dependent Claims 2 and 4

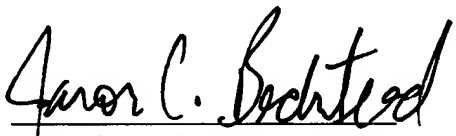
Dependent claims 2 and 4 are averred to be patentable at least by virtue of their dependence upon their respective base claims, in addition to their individual recitations.

II. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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Date: June 24, 2003

APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The specification is changed as follows:

The formula at the top of page 21 is changed as noted below (please note that a "2" ("two") is added next to the "beta" symbol):

$$Vs = \frac{V1 + V2}{2} - \sqrt{\frac{Io}{2\beta}} - Vth \qquad (25)$$

The following is added immediately after formula (25) on page 21:

This is equivalent to the notation: $V_s=(V_1+V_2)/2 - \sqrt{[I_0/(2\beta)]} - V_{TH}$, and shows that the common source voltage Vs includes a constant offset voltage:

$-\sqrt{[I_0/(2\beta)]}-V_{TH.}$.